# Enhanced VLSI Architecture of Partial Product Generator using Redundant Binary Modified Partial Product Generator Method

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**Abstract – Adders are the key component of the arithmetic unit, particularly quick parallel addition. Redundant Binary Signed Digit (RBSD) adders are intended to perform high-speed arithmetic operations. For the most part, in a high radix adjusted Booth encoding calculation partial products are lessened in augmentation process. A redundant Binary (RB) representation can be utilized when designing high performance multipliers, because of its high measured quality and convey free option, The traditional RB multiplier re quires an extra RB partial product (RBPP) row, on the grounds that error correcting word (ECW) is created by both the radix-4 Modified Booth encoding (MBE) and the RB encoding. This brings about in an extra RBPP accumulation stage for the MBE multiplier. Another RB altered partial product generator RBMPPG is proposed; it expels the additional ECW and consequently, it spares one RBPP RBPP accumulation stage. In this way, the proposed RBMPPG creates less halfway item pushes than a regular RB MBE multiplier. Simulation results show that the proposed RBMPPG generates fewer partial product rows than a conventional RB MBE multiplier. Simulation results show that the proposed RBMPPG based designs significantly improve the area and power consumption when the word length of each operand in the multiplier is at least 32 bits.**

**Index Terms – Redundant binary, modified Booth encoding, RB partial product generator, RB multiplier.**

## 1. INTRODUCTION

The advanced multiplier is a pervasive math unit in chip, computerized flag processors, and developing media processors. It is likewise a bit administrator in application particular information way of video and sound codes, advanced channels, PC illustrations, and installed frameworks. Contrasted and numerous other number juggling operations, increase is tedious and control hungry. The basic ways ruled by computerized multipliers regularly force a speed restrain on the whole outline. Consequently, VLSI plan of rapid multipliers, with low vitality dispersal, is as yet a well known research subject. Repetitive twofold (RB) portrayal is one of the marked digit portrayals initially presented by Avizienis [9] in 1961 for quick parallel number juggling. Numerous calculations and models have been proposed to outline rapid and low-control multipliers [1-13]. A typical paired (NB) augmentation by advanced circuits incorporates three stages. In the initial step, incomplete items are created; in the second step, every single halfway item are included by a fractional item diminishment tree until the point when two incomplete item pushes remain. In the third step, the two incomplete item pushes are included by a quick convey proliferation snake. Two strategies have been utilized to play out the second step for the halfway item diminishment. A first technique utilizes 4-2 compressors, while a moment strategy utilizes repetitive twofold (RB) numbers. The two techniques permit the fractional item diminishment tree to be lessened at a rate of 2:1. The RB expansion is convey free, making it a promising substitute for two's supplement multi-operand expansion in a tree-organized multiplier. Like an ordinary parallel (NB) multiplier, a RB multiplier is examined into three phases and comprises of four modules: the Booth encoder, RB fractional item generator (otherwise called decoder), RB incomplete item aggregator, and RB-to-NB converter. A Radix-4 Booth encoding or an adjusted Booth encoding (MBE) is generally utilized as a part of the halfway item generator of parallel multipliers to decrease the quantity of fractional item pushes considerably [5-6] [10-13]. A RBPP column can be acquired from two adjoining NB halfway item pushes by modifying one of the combine lines [5-6]; a N-bit tradition al RB MBE (CRBBE-2) multiplier requires N/4 RBPP lines. An extra mistake redressing word (ECW) is additionally required by both the RB and the Booth encoding [5-6] [14]; in this way, the quantity of RBPP gathering stages (NRBPPAS) required by an energy of-two word-length (i.e., 2 - bit) multiplier is given by: NRBPPAS = log ( N/4 + 1)

= n − 1, if N = 2^n.

This paper concentrates on the RBPP generator for planning a 2 - bit RB multiplier with less fractional item pushes by taking out the additional ECW. Another RB changed incomplete item generator in view of MBE (RBMPPG-2) is proposed. In the proposed RBMPPG-2, the ECW of each column is moved to

its next neighbor push. Besides, the additional ECW created by the last halfway item push is joined with both the two most noteworthy bits (MSBs) of the principal incomplete item push and the two minimum critical bits (LSBs) of the last fractional item push by rationale disentanglement. In this manner, the proposed technique lessens the quantity of RBPP columns from N/4 + 1to N/4, i.e., a RBPP collection organize is spared. The proposed strategy is connected to 8×8-piece, 16×16-piece, 32×32-piece, and 64×64-piece RB multiplier plans; the outlines are orchestrated utilizing the NanGate 45nm Open Cell Library. The proposed outlines accomplish critical decreases in territory and power utilization contrasted and existing multipliers when the word length of each of the operands is no less than 32 bits.

## 2. LITERATURE SURVEY

A high-radix Booth encoding strategy can lessen the quantity of incomplete items. Be that as it may, the quantity of costly hard products (i.e., a numerous that is not an energy of two and the operation can't be per-framed by straightforward moving and additionally complementation) increments as well. Besli et al. seen that some hard products can be acquired by the distinctions of two basic energy of-two duplicates. Another radix-16 Booth en-coding (RBBE-4) procedure without ECW has been expert postured, it evades the issue of hard products. A radix-16 RB Booth encoder can be utilized to beat the hard numerous issue and stay away from the additional ECW, yet at the cost of multiplying the quantity of RBPP columns. In this way, the quantity of radix-16 RBPP lines is the same as in the radix-4 MBE. Be that as it may, the RBPP generator in view of a radix-16 Booth encoding has a mind boggling circuit structure and a lower speed contrasted and the MBE incomplete item generator while requiring a similar number of halfway items.

## 3. PROPOSED SYSTEM

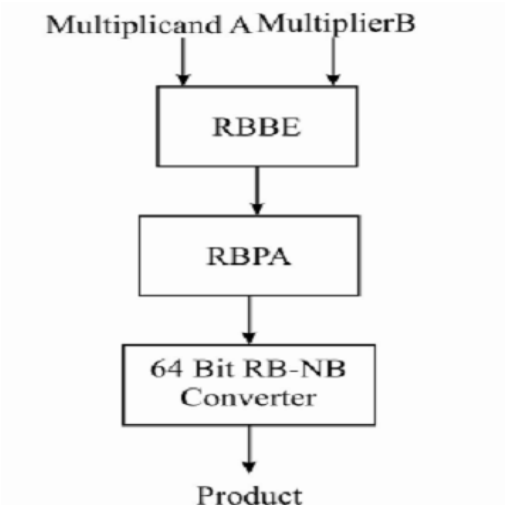



Fig.1.block diagram

The aim of this study is implementation of modified partial product generator for RB multipliers. A RB multiplier consists of a RB partial product (RBPP) generator, a RBPP diminishment tree and a RB-NB converter. A Radix-4 Booth encoding or an adjusted Booth encoding (MBE) is normally utilized as a part of the halfway item generator of parallel multipliers to decrease the quantity of incomplete item pushes by half.A RBPP column can be acquired from two neighboring NB fractional item pushes by transforming one of the combine lines.

Modified Booth Encoder

Keeping in mind the end goal to accomplish fast increase, duplication calculations utilizing parallel counters, for example, the changed Booth calculation has been proposed, and a few multipliers in view of the calculations have been executed for reasonable utilize. This kind of multiplier works significantly quicker than a cluster multiplier for longer operands since its calculation time is relative to the logarithm of the word length of operands.

Booth multiplication is a procedure that considers littler, speedier increase circuits, by recoding the numbers that are duplicated. It is conceivable to diminish the quantity of fractional items significantly, by utilizing the system of radix-4 Booth recoding. The essential thought is that, rather than moving and including for each segment of the multiplier term and increasing by 1 or 0, we just take each second segment, and duplicate by ±1, ±2, or 0, to acquire similar outcomes.

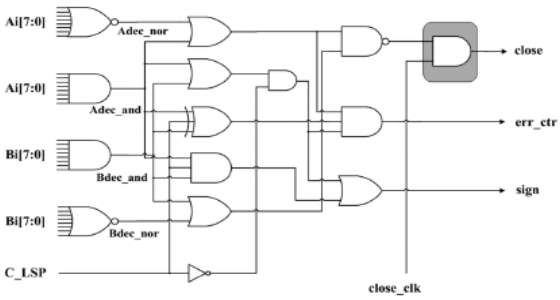



Fig 2. Modified Booth Encoder

The upside of this technique is the dividing of the quantity of incomplete items. To Booth recode the multiplier term, we consider the bits in pieces of three, to such an extent that each square covers the past piece by one piece. Gathering begins from the LSB, and the principal piece just uses two bits of the multiplier. Figure 3 demonstrates the gathering of bits from the multiplier term for use in adjusted corner encoding.

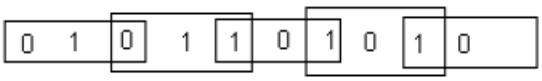



Fig.3 Grouping of bits from the multiplier term

Each block is decoded to generate the correct partial product. The encoding of the multiplier Y, using the modified booth algorithm, generates the following five signed digits, -2, -1, 0, +1, +2. Each encoded digit in the multiplier performs a certain operation on the multiplicand, X, as illustrated in Table 1

Table 1

| Block | Re-coded digit | Operation on X |
|---|---|---|
| 000 | 0 | 0 X |
| 001 | +1 | +1 X |
| 010 | +2 | +2 X |
| 011 | +2 | +2 X |
| 100 | -2 | -2 X |
| 101 | -1 | -1 X |
| 110 | -1 | -1 X |
| 111 | 0 | 0 X |

For the fractional item era, we embrace Radix-4 Modified Booth calculation to diminish the quantity of incomplete items for around one half. For duplication of 2"s supplement numbers, the no-account encoding utilizing this calculation filters a triplet of bits. At the point when the multiplier B is isolated into gatherings of two bits, the calculation is connected to this gathering of separated bits. Figure 4, demonstrates a processing case of Booth increasing two numbers "2AC9" and "006A". The shadow indicates that the numbers in this piece of Booth duplication are each of the zero with the goal that this piece of the calculations can be disregarded. Sparing those calculations can fundamentally diminish the power utilization caused by the transient signs. As indicated by the examination of the duplication appeared in figure 4, we propose the SPST-prepared altered Booth encoder, which is controlled by a recognition unit. The discovery unit has one of the two operands as its contribution to choose whether the Booth encoder ascertains repetitive calculations. As appeared in figure 9. The hooks can, individually, solidify the contributions of MUX-4 to MUX-7 or just those of MUX-6 to MUX-7 when the PP4 to PP7 or the PP6 to PP7 are zero; to diminish the change control scattering. Figure 10, demonstrates the stall halfway item era circuit. It incorporates AND/OR/EX-OR rationale.

RB Partial Product Generator:

As two bits are used to represent one RB digit, then a RBPP is generated from two NB partial products [1-6]. The addition of two N-bit NB partial products X and Y using two's complement representation can be expressed as follows X +Y = X –Y -1 = (X ,Y-) -1.

Where Y- is the inverse of Y. The RBPP is generated by inverting one of the two NB partial products and adding -1 to the LSB. Each RB digit X ibelongs to the set{-1,0,1};this is coded by two bits (Xi-, Xi+) .RB numbers can be coded in several ways.

TABLE 2

RB Encoding Scheme

| $X_i^+$ | $X_i^-$ | RB digit $(X_i)$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | $\bar{1}$ |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Both MBE and RB coding schemes introduce errors and two correction terms are required: 1) when the NB number is converted to a RB format, -1 must beaddedto the LSB of the RB number; 2) when the multiplicand is multiplied by -1 or - 2 during the Booth encoding, the number is inverted and +1 must be added to the LSB of the partial product. A single ECW can compensate errors from both the RB encoding and the radix-4 Booth recoding.

Proposed RB Partial ProductGenerator:

A new RB modified partial product generator based on MBE (RBMPPG-2) is presented in this section; in this design, ECW is eliminated by incorporating it into both the two MSBs of the first partial product row (PP 1+ ) andthe two LSBs of the last partial product row (PP – (N/4)).

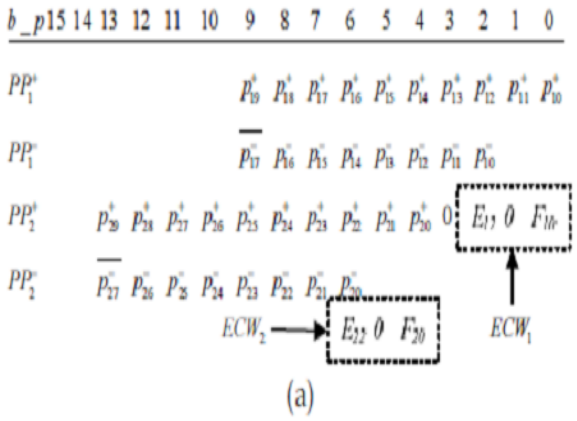



Fig.4(a)The first new RBMPPG-2 architecture for an 8-bit MBmultiplier

It is differ from conventional type by its error correcting vector. In this type error correcting vectors ECW1 is generated by PP1 and ECW 2 is generated by PP2.

ECW1= 0 E12 0 F 10
ECW2= 0 E 22 0 F 20

To eliminate a RBPP accumulation, ECW 2 needs to be incorporated into PP1 and PP2.
F20={-1 , b5 b4 b3=000,001,010,011,111
F20={0 , b 5b4b3=100,101,110

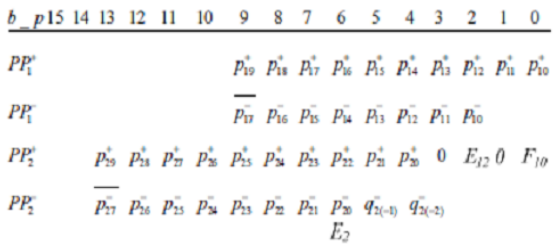


Fig 4(b)Revised RBMPPG by replacing E22and F20

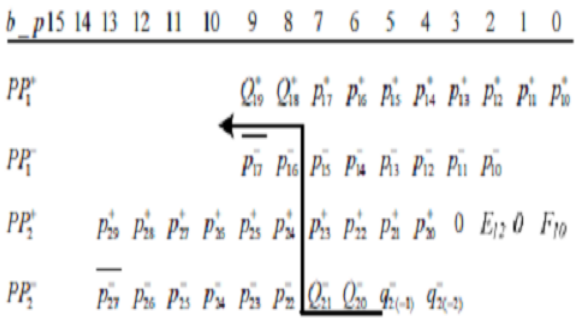


Fig4(c) final proposed RBMPPG by totally eliminating ECW2

Q 19+ ,Q 18+,Q 21-,Q20- are used to represent the modified partialproducts .By setting PP2+ to all ones and adding +1 to theLSB of the partial product ,F20 can then be determined only by b5

F20={-1, b5=0
F 20= {0, b5 =1

As -1 can be coded as 111 in RB format,E 22 and F 20 can berepresented by E 2 ,q 2(-2-) ,q 2(-1)- as follows

$$E_2 = \begin{cases} E_{22}, & F_{20} = 0 \\ E_{22} - 1, & F_{20} = -1 \end{cases}$$

$$q_{2(-2)}^- = q_{2(-1)}^- = \begin{cases} 0, & F_{20} = 0 \\ 1, & F_{20} = -1 \end{cases}$$

This is further explained by the truth table ofE22,F20 and E2, q2-(-2),q2-(-1) .

TABLE 3

TRUTH TABLE OF $E_2$, $q_{2(-2)}^-$, $q_{2(-1)}^-$ AND $p_{21}^-$,$p_{20}^-$.

| $b_7b_6b_5$ | $E_{22}F_{20}$ | $E_2q_{2(-2)}^-q_{2(-1)}^-$ | $p_{21}^-$ | $p_{20}^-$ |
|---|---|---|---|---|
| 0 0 0 | 0 $\bar{1}$ | $\bar{1}$ 1 1 | 0 | 0 |
| 0 0 1 | 0 0 | 0 0 0 | $a_1$ | $a_0$ |
| 0 1 0 | 0 $\bar{1}$ | $\bar{1}$ 1 1 | $a_1$ | $a_0$ |
| 0 1 1 | 0 0 | 0 0 0 | $a_0$ | 0 |
| 1 0 0 | 1 $\bar{1}$ | 0 1 1 | $\overline{a_0}$ | 1 |
| 1 0 1 | 1 0 | 1 0 0 | $\overline{a_1}$ | $\overline{a_0}$ |
| 1 1 0 | 1 $\bar{1}$ | 0 1 1 | $\overline{a_1}$ | $\overline{a_0}$ |
| 1 1 1 | 0 0 | 0 0 0 | 0 | 0 |

The relationships between Q 19+ ,Q 18+,Q 21-,Q20- and P19+,P21-,P20- are summarized in table.

THE TRUTH TABLE OF $Q_{19}^+$, $Q_{18}^+$, $Q_{21}^-$, $Q_{20}^-$

| $p_{19}^+p_{18}^+p_{21}^-p_{20}^-$ | $Q_{19}^+Q_{18}^+Q_{21}^-Q_{20}^-$ ($E_2$=0) | $Q_{19}^+Q_{18}^+Q_{21}^-Q_{20}^-$ ($E_2$=1) | $Q_{19}^+Q_{18}^+Q_{21}^-Q_{20}^-$ ($E_2$= −1) |
|---|---|---|---|
| 0100 | 0100 | 0101 | 0011 |
| 0101 | 0101 | 0110 | 0100 |
| 0110 | 0110 | 0111 | 0101 |
| 0111 | 0111 | 1000 | 0110 |
| 1000 | 1000 | 1001 | 0111 |
| 1001 | 1001 | 1010 | 1000 |
| 1010 | 1010 | 1011 | 1001 |
| 1011 | 1011 | 1100 | 1010 |

Logic functions of Q19+,Q18+,Q21-and Q20- can be expressedas follows

$$Q_{19}^+ = (b_7 \oplus b_5 + b_7b_6b_5) \cdot p_{19}^+ + \overline{b_7}\,\overline{b_5} \cdot (p_{18}^+ + p_{21}^- + p_{19}^+) + b_7\overline{b_6}b_5 \cdot (p_{18}^+p_{21}^-p_{20}^- \oplus p_{19}^+)$$

$$Q_{18}^+ = (b_7 \oplus b_5 + b_7b_6b_5) \cdot p_{18}^+ + \overline{b_7}\,\overline{b_5} \cdot (\overline{p_{21}^- + p_{20}^-} \oplus p) + b_7\overline{b_6}b_5 \cdot (p_{21}^-p_{20}^- \oplus p_{18}^+)$$

$$Q_{21}^- = (b_7 \oplus b_5 + b_7b_6b_5) \cdot p_{21}^- + \overline{b_7}\,\overline{b_5} \cdot \overline{p_{21}^- \oplus p_{20}^-} + b_7\overline{b_6}b_5 \cdot p_{21}^- \oplus p_{20}^-$$

$$Q_{20}^- = (b_7 \oplus b_5 + b_7b_6b_5) \cdot p_{20}^- + \overline{b_7}\,\overline{b_5} \cdot \overline{p_{20}^-} + b_7\overline{b_6}b_5 \cdot \overline{p_{20}^-}$$

Therefore, the extra ECW N/4 is removed by the transformation of 4 partial product variables and one partial product row is saved in RB multipliers with any power-of-two word-length.

RBPA

In the second stage, a 4-stage RBA summing tree is used to sum 16 RB partial products. Each RBA block contains 64 RB full adder (RBFA) cells and a varying number of RB half adder (RBHA) cells depending on where it is located. The proposed RBMPPG-2 can be applied to any bit RB multipliers with a reduction of a RBPP accumulation stage compared with conventional designs. Although the delay of RMPPG-2 increases by 1-stage of TG delay, the delay of one RBPP accumulation stage is significantly larger than a 1-stage TG delay. Therefore, the delay of the entire multiplier is reduced. The improved complexity, delay and power consumption are very attractive for the proposed design. The multiplier consists of the proposed RBMPPG-2, three RBPP accumulation stages, and one RB-NB converter. Eight

RBBE-2 blocks generate the RBPP they are summed up by the RBPP reduction tree that has three RBPP accumulation stages. Each RBPP accumulation block contains RB full adders (RBFAs) and half adders (RBHAs).


Fig. 5. The block diagram of a 32-bit RB multiplier using the proposed RBMPPG-2.

The proposed RBMPPG-2 can be connected to any 2n-bit RB multipliers with a decrease of a RBPP aggregation arrange contrasted and regular outlines. Despite the fact that the postponement of RMPPG-2 increments by one-phase of TG delay, the deferral of one RBPP aggregation arrange is essentially bigger than a one-organize TG delay. Along these lines, the deferral of the whole multiplier is decreased. The enhanced multifaceted nature, postponement and power utilization are exceptionally alluring for the proposed plan.

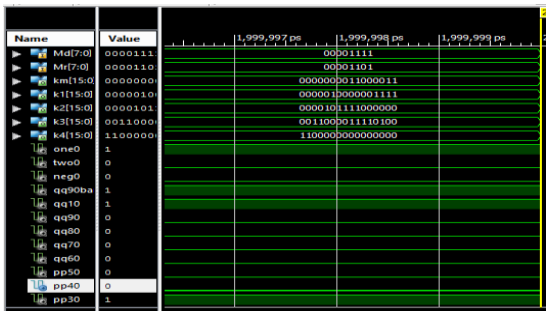
A 32-bit RB MBE multiplier utilizing the proposed RBPP generator is appeared in Fig. 5. The multiplier comprises of the proposed RBMPPG-2, three RBPP aggregation stages, and one RB-NB converter. Eight RBBE-2 pieces create the RBPP (pþi , p i ); they are summed up by the RBPP diminishment tree that has three RBPP gathering stages. Each RBPP gathering piece contains RB full adders (RBFAs) and half adders (RBHAs) [7]. The 64-bit RB-NB converter changes over the last collection comes about into the NB portrayal, which utilizes a half and half parallel-prefix/convey select viper [25] (as a standout amongst the most productive quick parallel snake plans).

There are four phases in a traditional 32-bit RB MBE multiplier engineering; in any case, by utilizing the proposed RBMPPG-2, the quantity of RBPP aggregation stages is decreased from 4 to 3 (i.e., a 25 percent lessening). These are critical funds in delay, zone and also control utilization. The upgrades in postponement, zone and power utilization are additionally exhibited in the following area by recreation.

## 4. RESULTS

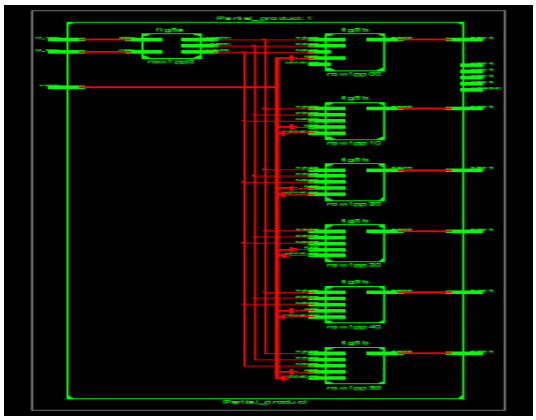
The written Verilog HDL Modules have successfully simulated and verified using Model sim III 6.4b and synthesized using Xilinx ISE 13.2

Simulation Result:

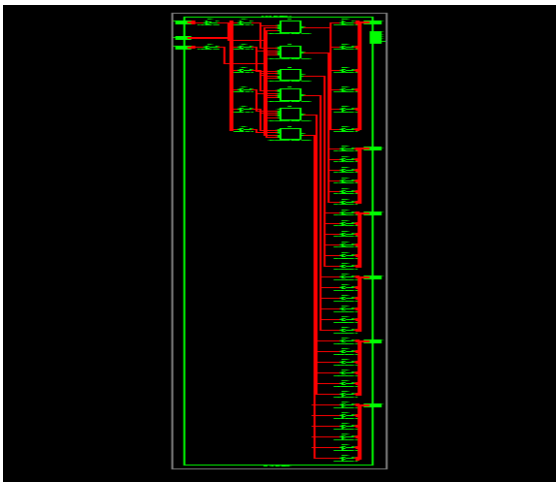



Synthesis Results:

RTL Schematic:



Technology Schematic:



## 5. CONCLUSION

A new modified RBPP generator has been proposed in this paper; this design eliminates the additional ECW that is introduced by previous designs. Therefore, a RBPP accumulation stage is saved due to the elimination of ECW. The new RB partial product generation technique can be applied to any 2n-bit RB multipliers to reduce the number of RBPP rows from N/4 + 1 to N/4. Simulation results have shown that the performance of RB MBE multipliers using the proposed RBMPPG-2 is improved significantly in terms of delay and area. The proposed designs achieve significant reductions in area and power consumption when the word length is at least 32 bits.

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